Patent

#29
Declaration
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FJONES
1-8-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Vora

Art Unit: 2811

Examiner: S. Crane

Serial No. 08/654,760

Filed: May 29, 1996

For: VERTICALLY INTEGRATED FLASH EEPROM FOR GREATER DENSITY AND LOWER COST

Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

Morgan Hill, California
December 16, 2002

DECLARATION OF MADHU VORA UNDER 37 CFR 1.132

Dear Sir:

Being hereby warned that willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. 1001) and may jeopardize the validity of the application or any patent issuing thereon, I hereby voluntarily make the following statements. The following statements made of my own knowledge are true, and all statements made on information and belief are believed to be true.

My name is Madhukar Vora. I am the inventor on the above identified patent application. I received a BSEE from the Government Engineering College in India in 1961. I received a masters degree in electrical engineering from Worcester Polytechnic Institute in 1962. My first job was with IBM where I specialized in semiconductor device design, semiconductor device physics, construction and device modelling. I worked at IBM on semiconductor devices and processes from 1962 to 1977. I obtained about 35-40 patents during my time at IBM as I recall. I then joined Fairchild Cameral and Instrument in the Palo Alto advanced research center where I specialized

in semiconductor device design, device physicsm modelling and semiconductor integrated circuit process development. I worked at Fairchild from 1977 to 1987. I obtained a large number of patents while working at Fairchild, and I believe I have approximately 55 patents when I left Fairchild. I have been working in semiconductor design design companies ever since leaving Fairchild.

I analyzed the Otani et al. patent (5,786,612) and compared it to my invention and to the state of the art flash memory design by Samsung. My analysis is attached hereto as Exhibit 1, pages 1-32. This analysis shows how the key structural features of my invention of having a pipe or annulus floating gate along with drain regions on two sides of the well along the row which can be shared with neighboring cells on both sides, and self aligned contact holes to these drain areas for the bit lines make my cell much smaller than the Otani et al. cell. These drawings also show how the masks used in my invention to define the word line are not critical and show how misalignment of the word line mask is not fatal to the structure of my cell. I have also read everything Mr. Fish wrote in his amendment and studied the figures of Appendix A and I declare that these arguments are all well founded in fact and the drawings accurately depict the situations they illustrate. The reason Appendix A is missing page 2 and Figures A-3 and A-4 is that I made a mistake in what I told Mr. Fish and asked him to remove these figures.

Further, declarant sayeth not.

Dated: 12/11/02

Madhukar Vora

Vora Vs Otani Flash EPROM Patents Analysis

Key Structural Differences.

12/15/02

EXH. 1
PP. 1-32

The is most significant difference between Otani and Vora structures is the area of the cell. 12 F^2 Vs 4 F^2 based on Fig3 through Fig. 6, where F is the minimum feature size.

This vast difference in area is due to the some key structural innovations in Vora patent which do not exist in Otani Patent. The claim have to be written to cover these key structural innovations which are listed below.

1. In Vora Patent the Trench , where the EPROM Transistor is located, has all 4 sides surfaces of Silicon. Two adjacent trenches are separated by silicon (in D2 direction of Fig.5) as opposed to Otani Patent where trenches are separated by Oxide in D2 direction of Figure 3.

<u>Trench has 4 silicon sides in Vora. Trench has 2 silicon and oxide sides in Otani.</u>

2. The shape of the FG poly in Otani is a slab as in Fig 22 sticking to one side. The Shape of FG poly in Vora is like a square pipe as in Fig 20 and 22. Both top view and 3D view of FG poly for Otani and Vora are shown in Fig. 22.

FG is a slab in Otani and Square Pipe in Vora

3. The shape of FG poly has great significance in determining cell size. Vora Pipe allows one to build the transistors on both side of the trench in direction D1 of Figure 3. Otani Slab sticking to one side allows one toe to build only one transistor on one side since FG Poly is on only one side.

Otani has one transistor per trench. Vora has two transistor per trench

4. The N+ Drain diffusion is on one side of the trench in the Otani patent as in Fig. 3 and 21. That also is second reason why there is only one transistor per trench.. On the other hand Vora patent has N+ Drain diffusion on both side of the trench as in Fig 23 which is second reason why two transistor per trench are possible in Vora Patent.

Otani has N+ Diffusion on one side. Vora Has N+ Diffusion on Both Sides

5. The distance between two trenches in Otani is determined by the size of the metal contact (Which is min. feature size F.) and the distance between the edge of the contact and CG Poly (Which is also F). This alignment space F is needed because the uneven surface on which Contact oxide is deposited which is layer 21-1 in Fig.21.

6. The distance between two trenches in Fig 23 of Vora patent is 1F. Reason is that there is no separate contact hole defined by photolithography. The contact to N+ Drain is self aligned to CG Poly which is layer 23-2. This elimination of Photo defined Contact is major reason for reduction in space between drain and hence cell size.

Total space between two trenches is 3F in Otani and 1F in Vora.

6. CG Poly Layer 5-2 in Fig 5 serves three purposes. First one is to form a control gate 23-3. Second is to act as self aligned edges where contact by Bit line conductor is made to N+ drain silicon surface. Third is to form word line layer 24-1 in along section BB of Fig 24.. Details of construction in enlarged views is shown in Figures 7 – 12.

CG Poly is Control Gate, Self aligned Contact Edge and Word line

Note: Diagrams in 23 are turned by 90 degrees in diagram 24

8. Another feature the increases the density is the fact that Mask to form Word line, layer 5-2 of Fig 5 is non critical and is loosely aligned to trench. Width of Layer 5-2 is same as width of the trench. This Word line 5-2 of Fig 5 can be mis-aligned grossly still will perform its function of CG Electrode, Word-Line and provided and defining Edge for the contact of Bit Line Poly-Silicide to N+ Drain. To prove that mis-alignment of Poly layer 5-2 of Fig. 5 does not affect the transistor characteristics, two sets of drawings are drawn. First set Fig 7-12 shows perfectly aligned Poly layer5-2 of Fig. 5. Second set Fig 13- 18 shows grossly mis-aligned Word line layer 13-2 to trench layer 13-1. It can be seen from Fig 18 that Bit Line Poly Silicide 18-2 does not short with Bit Line Poly 18-3 or FG Poly 18-1

Word Line Poly (same as CG Poly) Mask is Non Critical in Vora. Word Line Poly Mask is Extremely critical in Otani.

8. The third poly layer 5with silicide is deposited to form a Bit line 5-1 that connects all the N+ Drain as Fig 5, 7, and Fig 23. This third poly Layer mask is non critical. On the other hand in Otani patent Bit Line Metal layer 3-2 to Contact hole, layer 3-1 in Fig.3 is very critical and space consuming.

In Vora third Poly is self aligned to Contacts to N+ Drain. In Otani Metal and Contact masks are not self aligned.

Summary: (1) Square Pipe FG, (2) Two sided Drain, (3) Self Aligned Contacts from using 2nd and 3rd poly and (4) Non critical 2nd and 3rd poly' masks enable area of the cell to be $4F^2$ in Vora Compared to Otani's 12 F^2.

State Of The Art Flash EPROM Cell

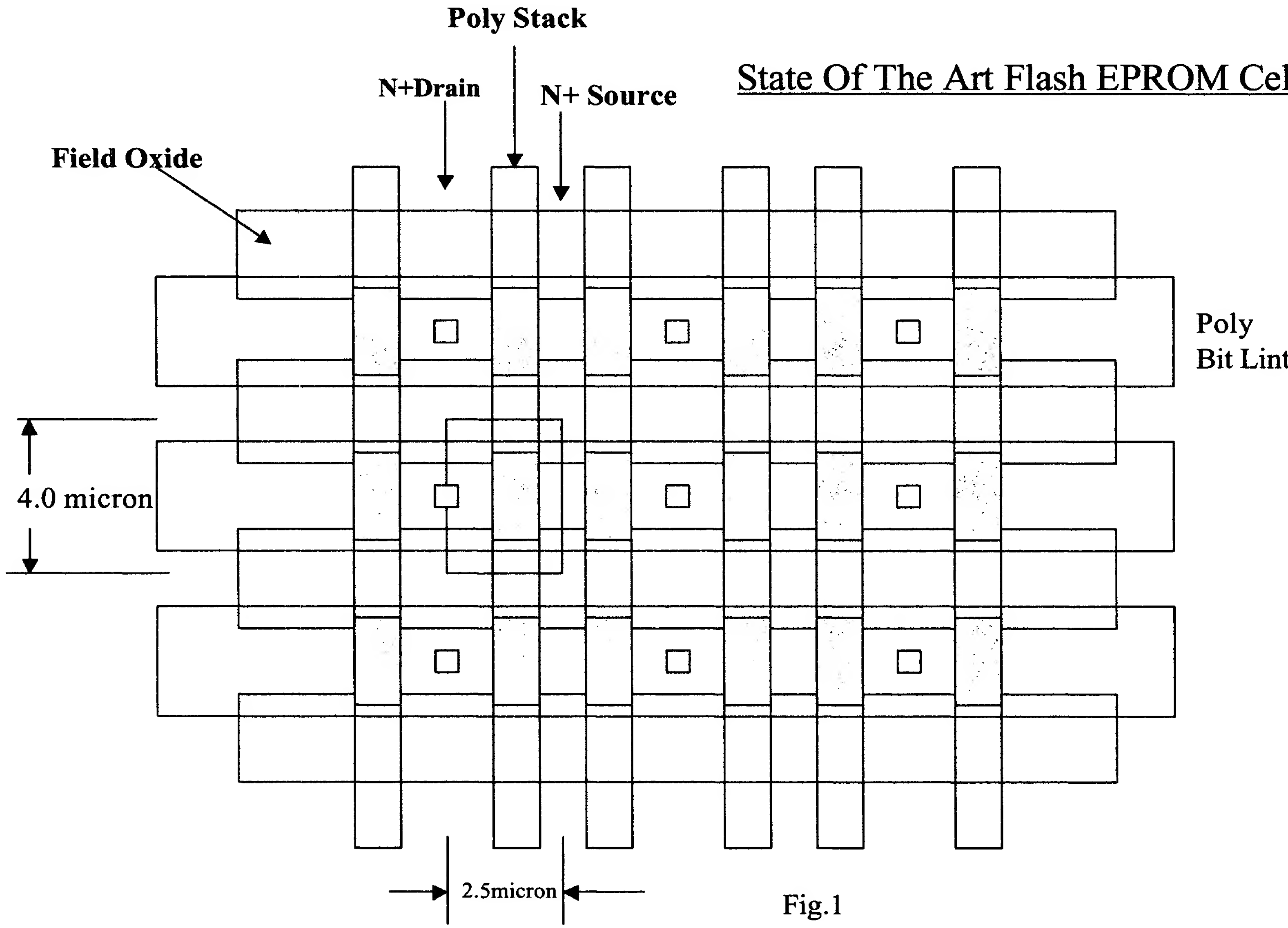


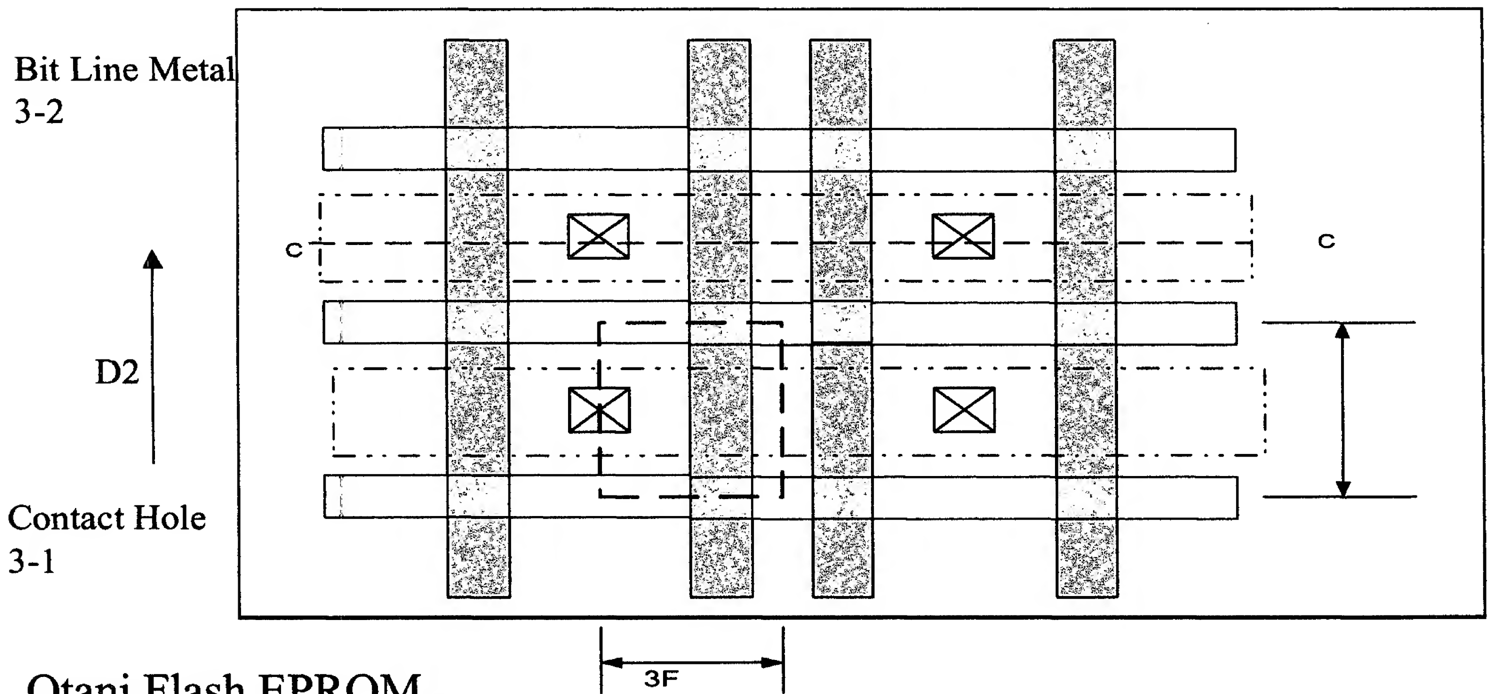
Fig.1

State Of The Art Flash EPROM Cell

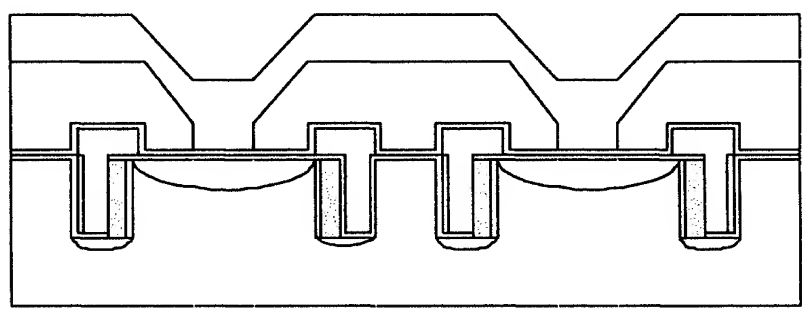
Cell Size:

Cell W = 2.5 F
Cell H = 4.0 F
Area = 10.0 F^2

Fig 2



Otani Flash EPROM



Section along CC of Top View above

Fig 3.

Otani Flash EPROM Cell

Cell Size:

Cell W = 3 F
Cell H = 4.0 F
Area = 12.0 F^2

Fig 4

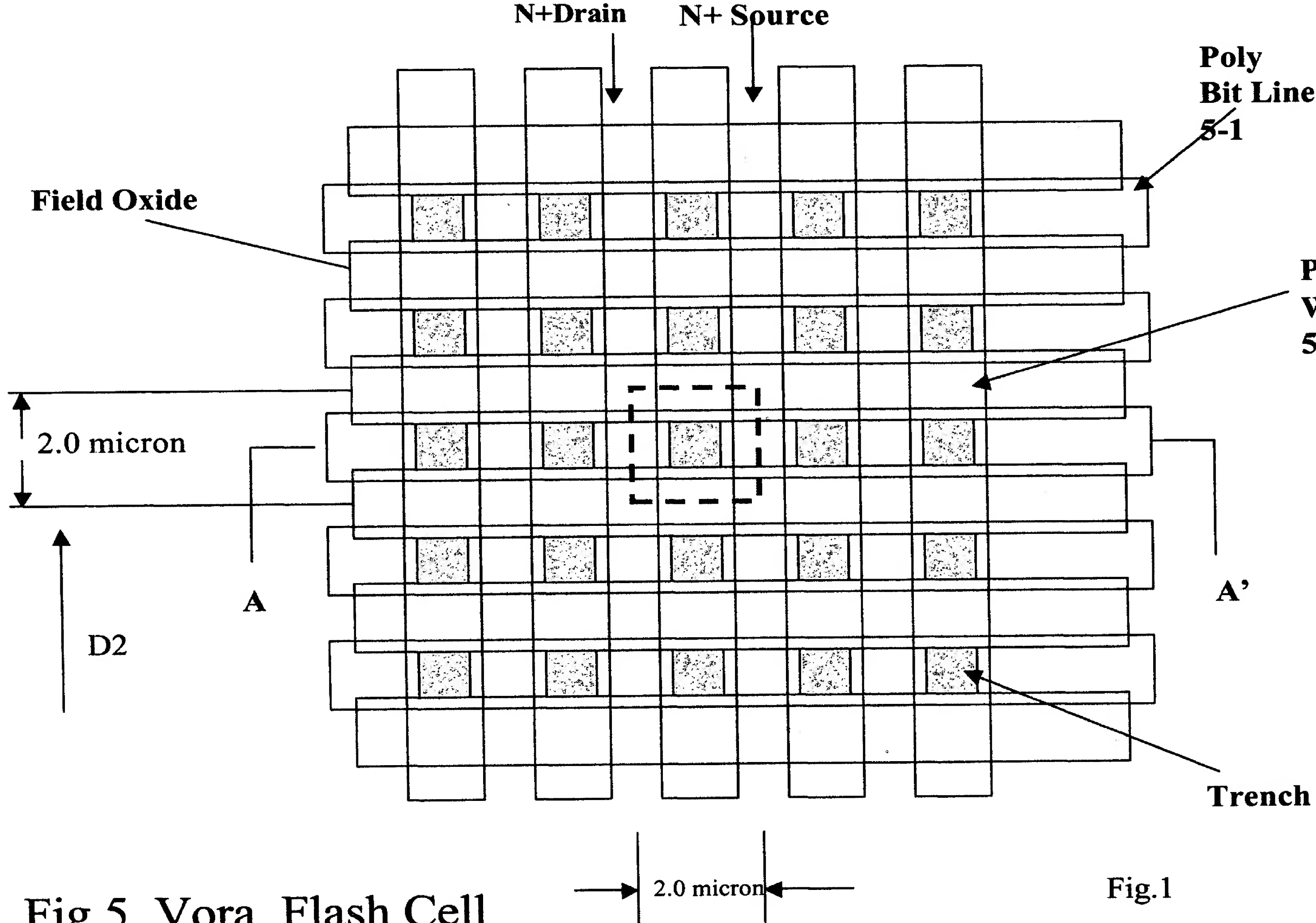


Fig.5. Vora Flash Cell

Vora Flash EPROM CELL

Cell Size:

Cell W = 2.0 F
Cell H = 2.0 F
Area = 4.0 F^2

Fig 6

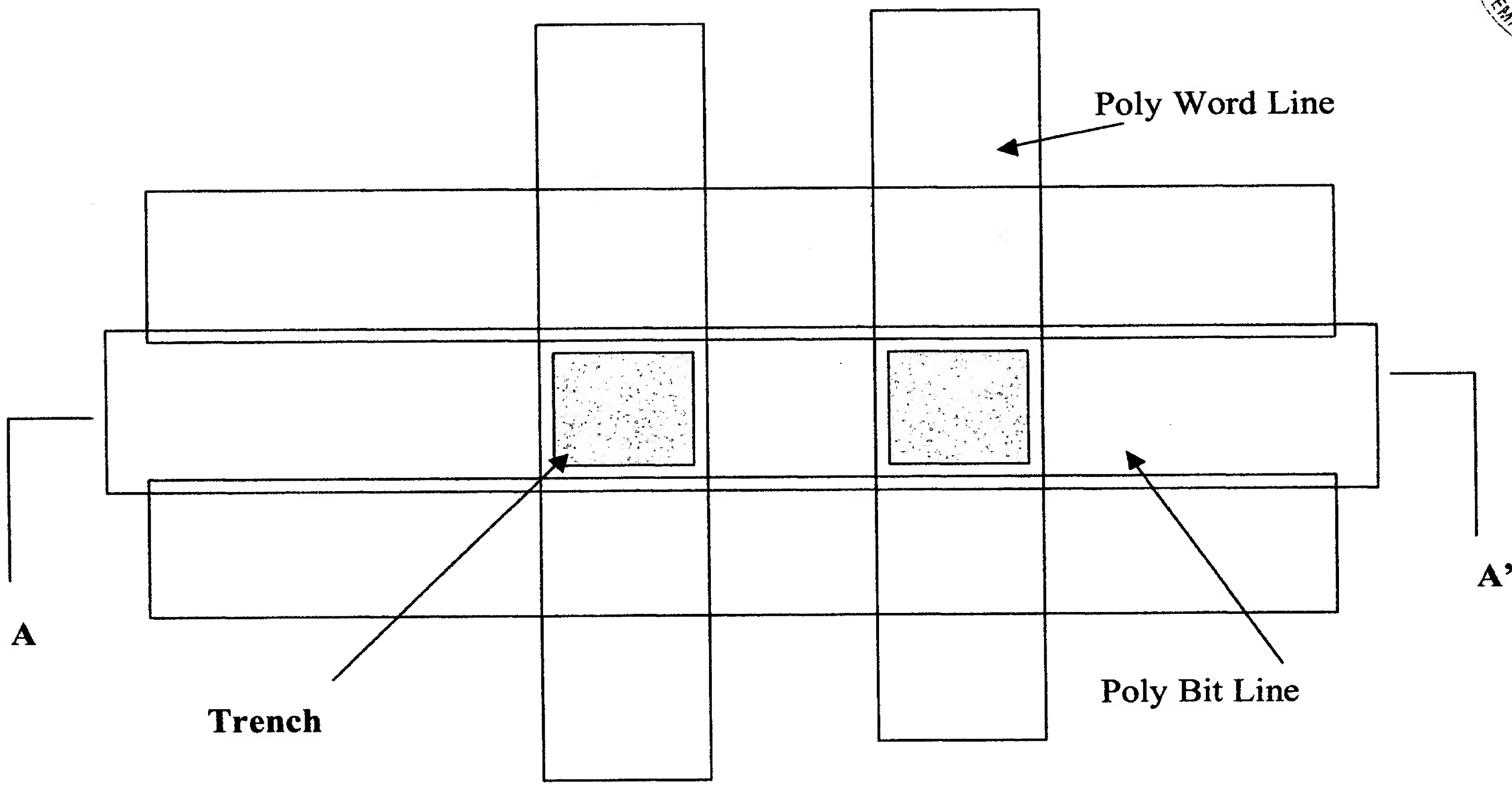


Fig 7. Flash EPROM Cell. Word Line aligned with Trench.

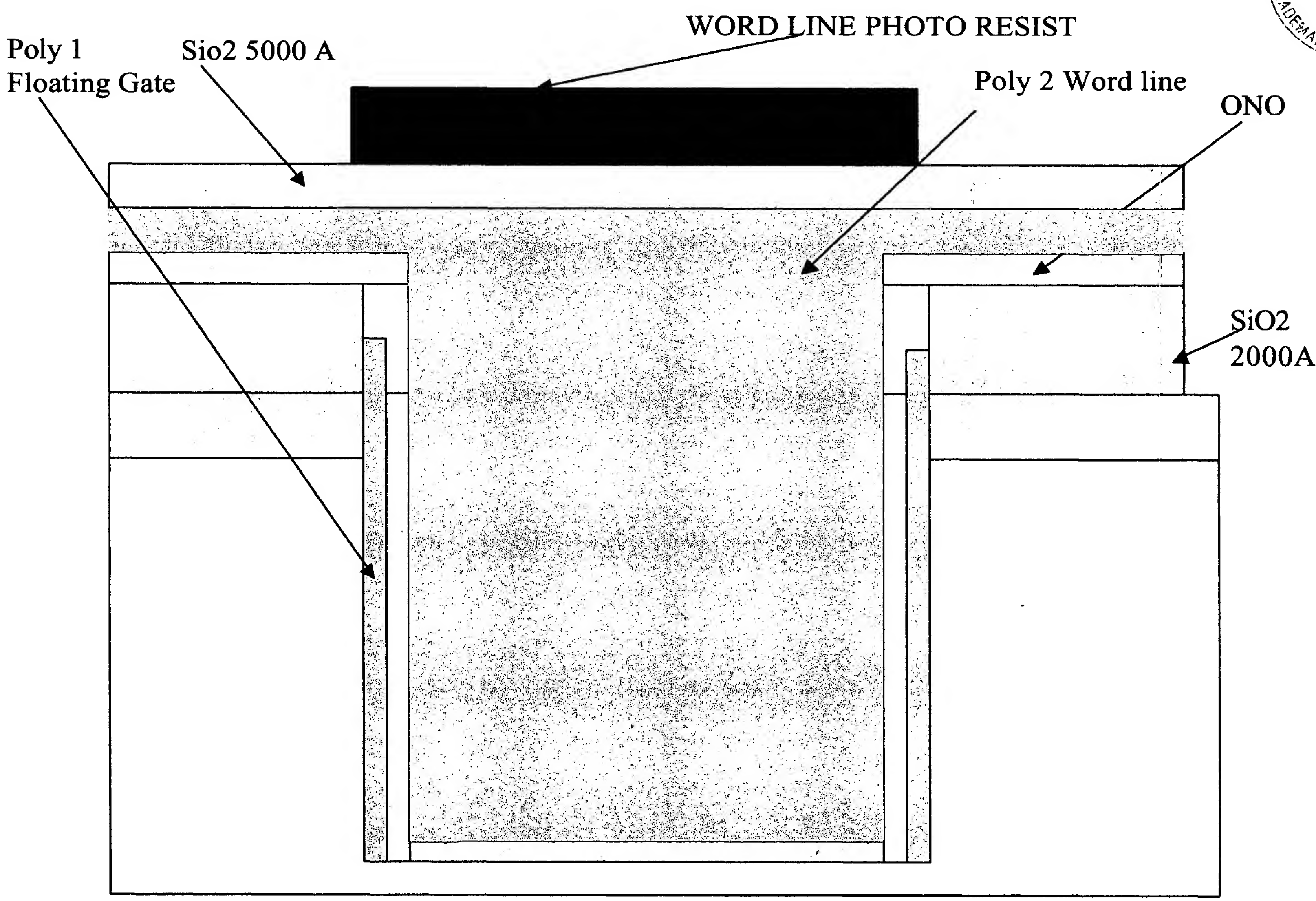


Figure 8. Cross section of Cell at AA' in Figure 2. Word line Photo resist Mis aligned .

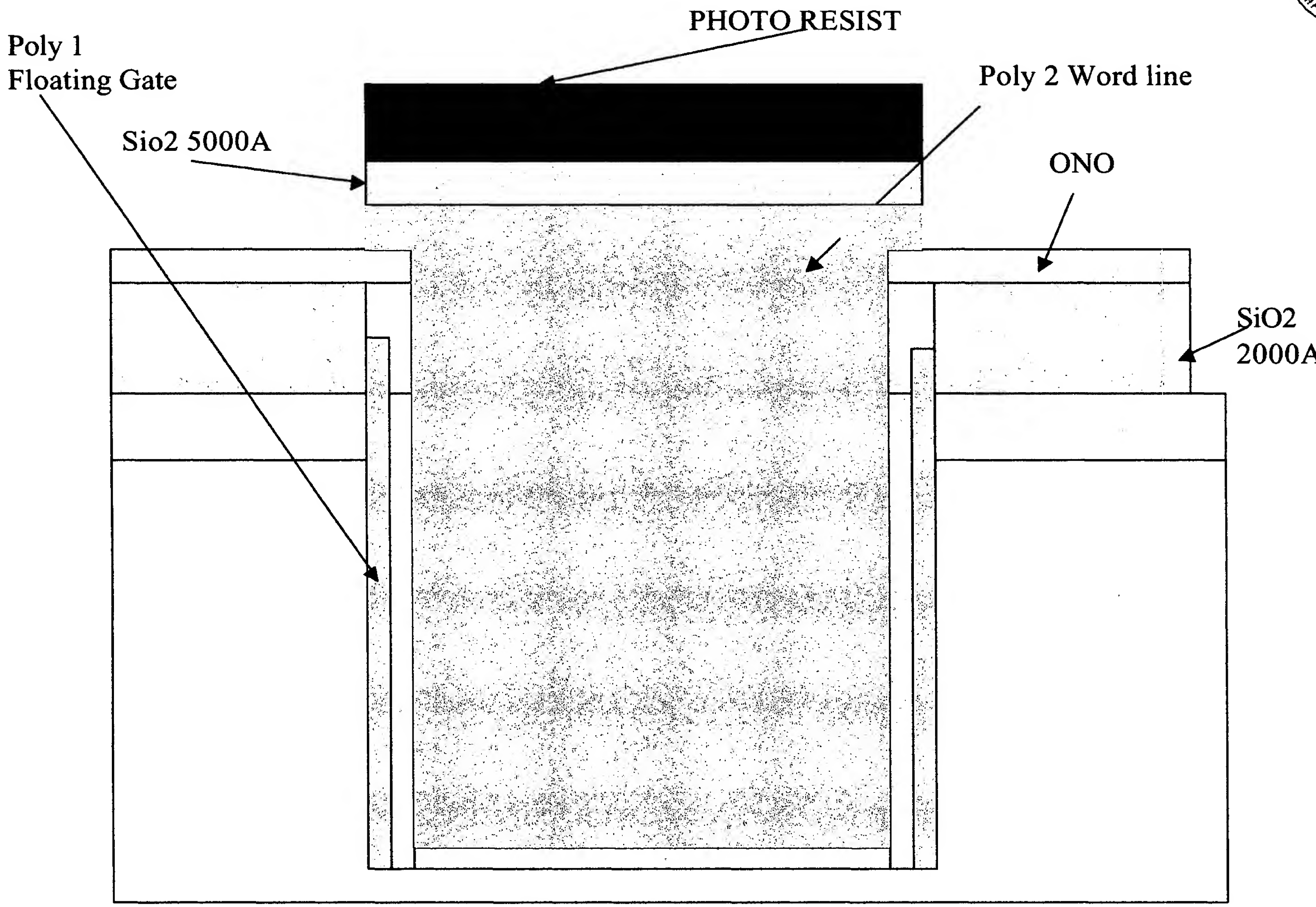


Fig.9. Oxide Etch

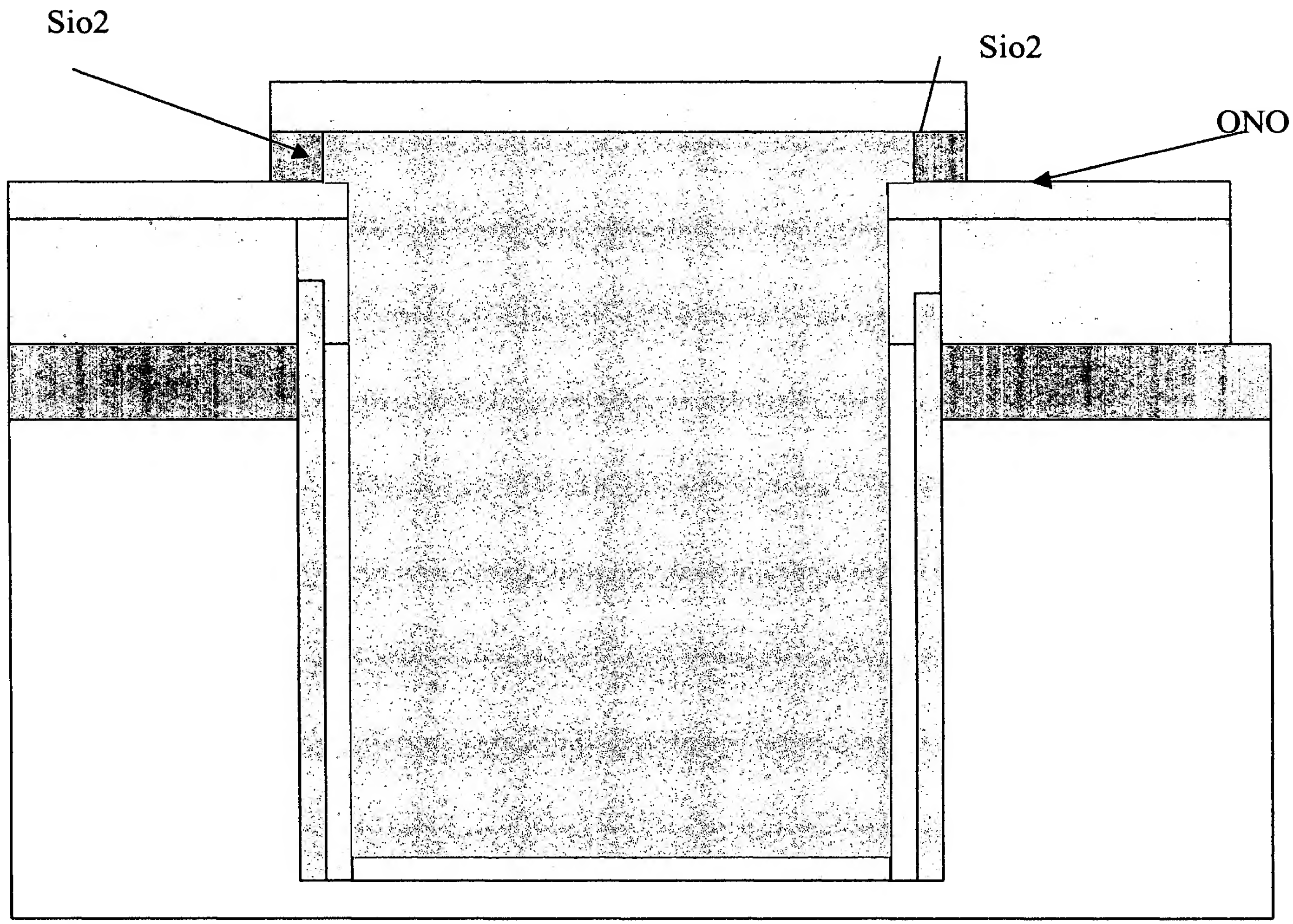


Fig. 10. Thermal Sio 2 Growth.

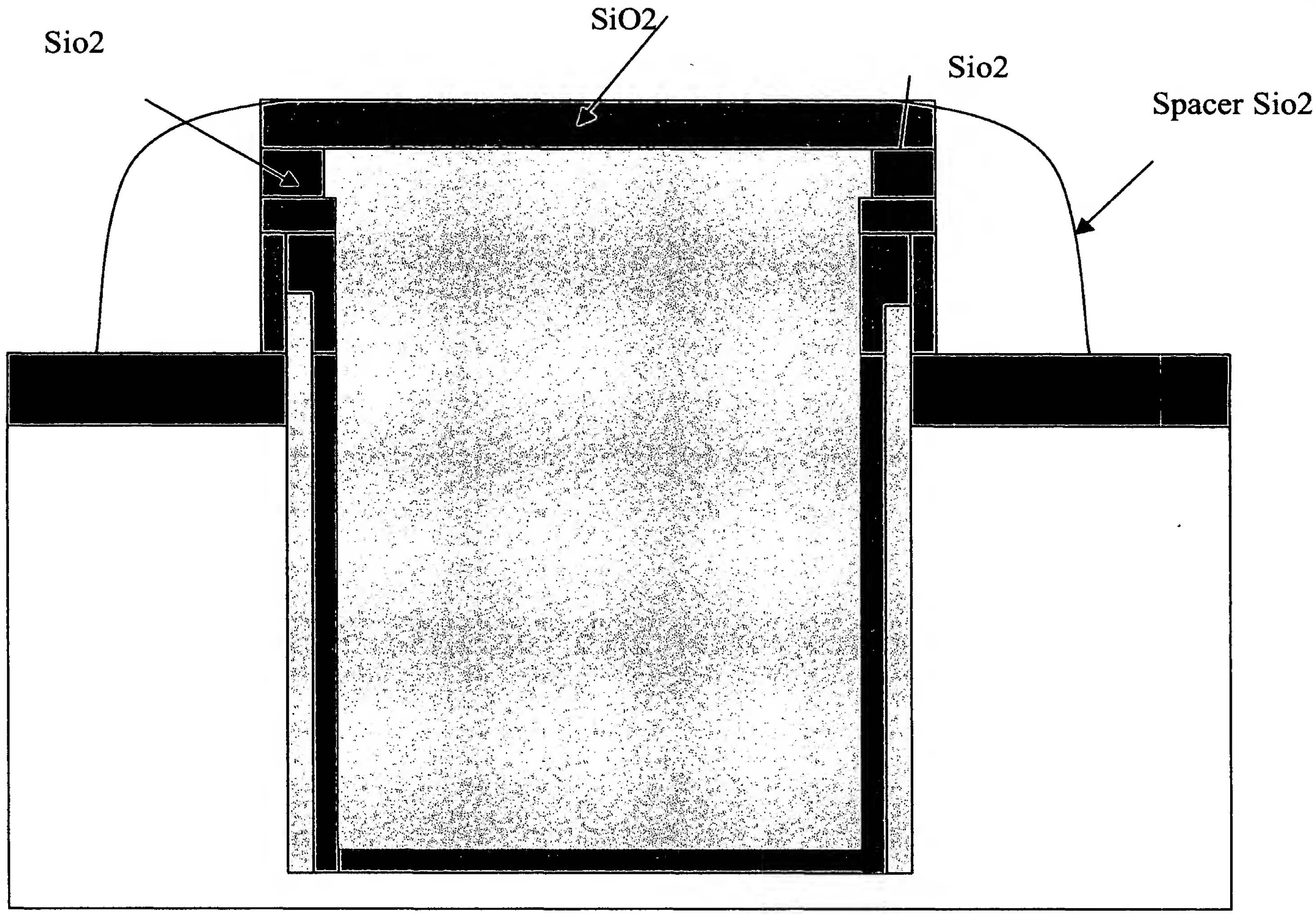


Fig.11. ONO etch, Oxide Etch. Spacer oxide (or ONO) Deposition. Anisotropic Oxide(or ONO) etch . to form Spacer

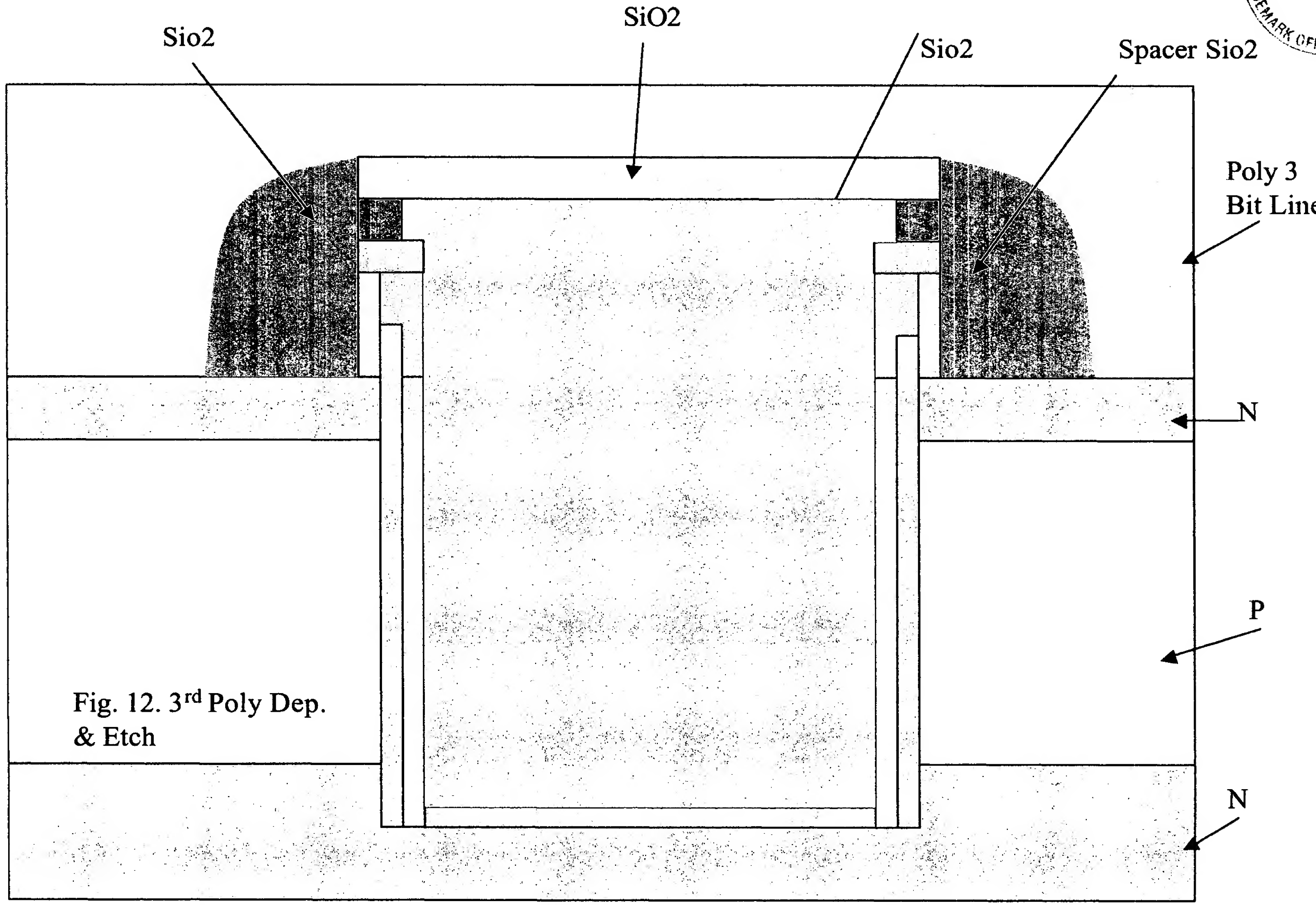


Fig. 12. 3rd Poly Dep. & Etch

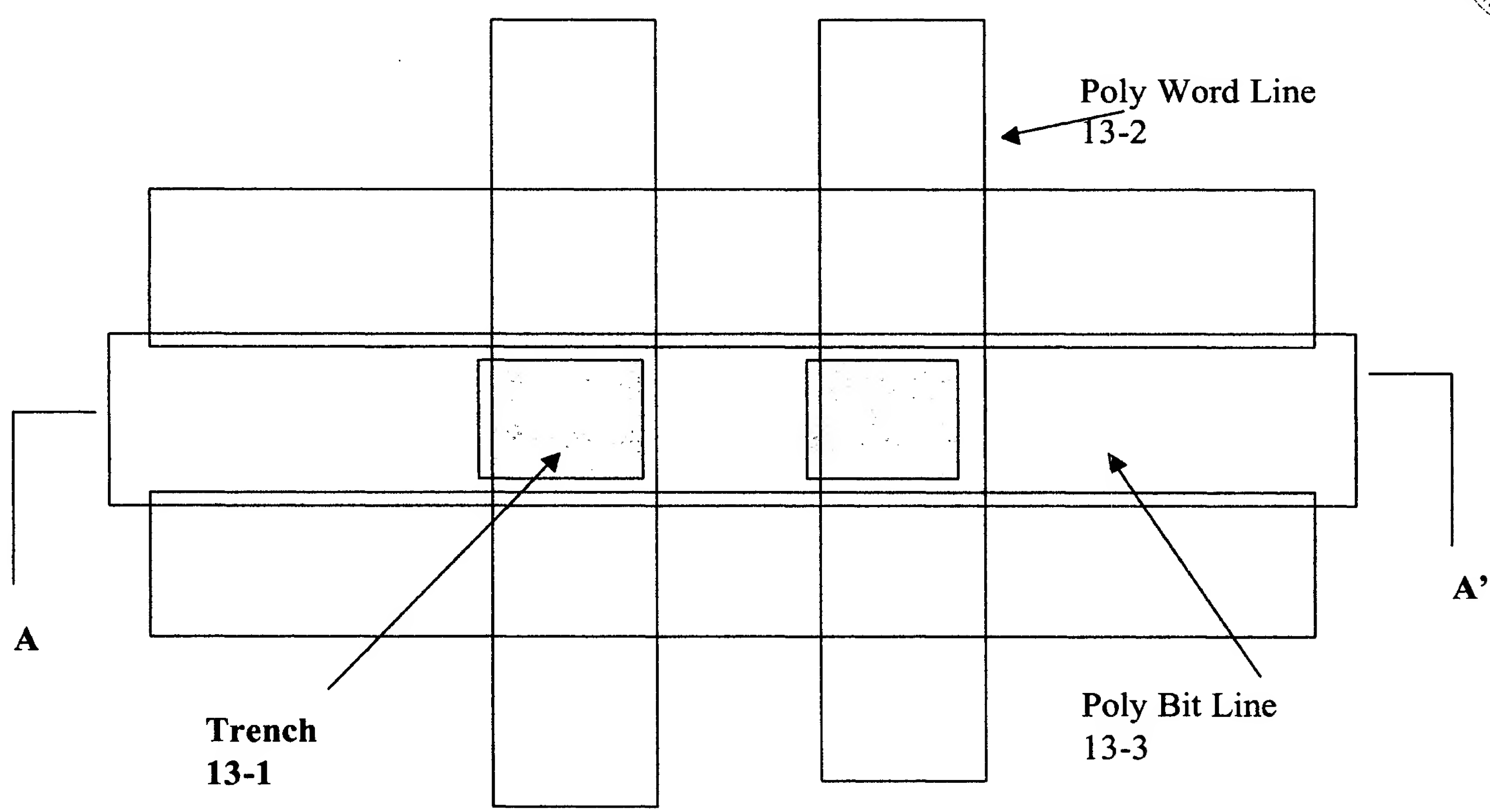


Fig.13. Flesh EPROM Cell. Word Line Misaligned with Trench.

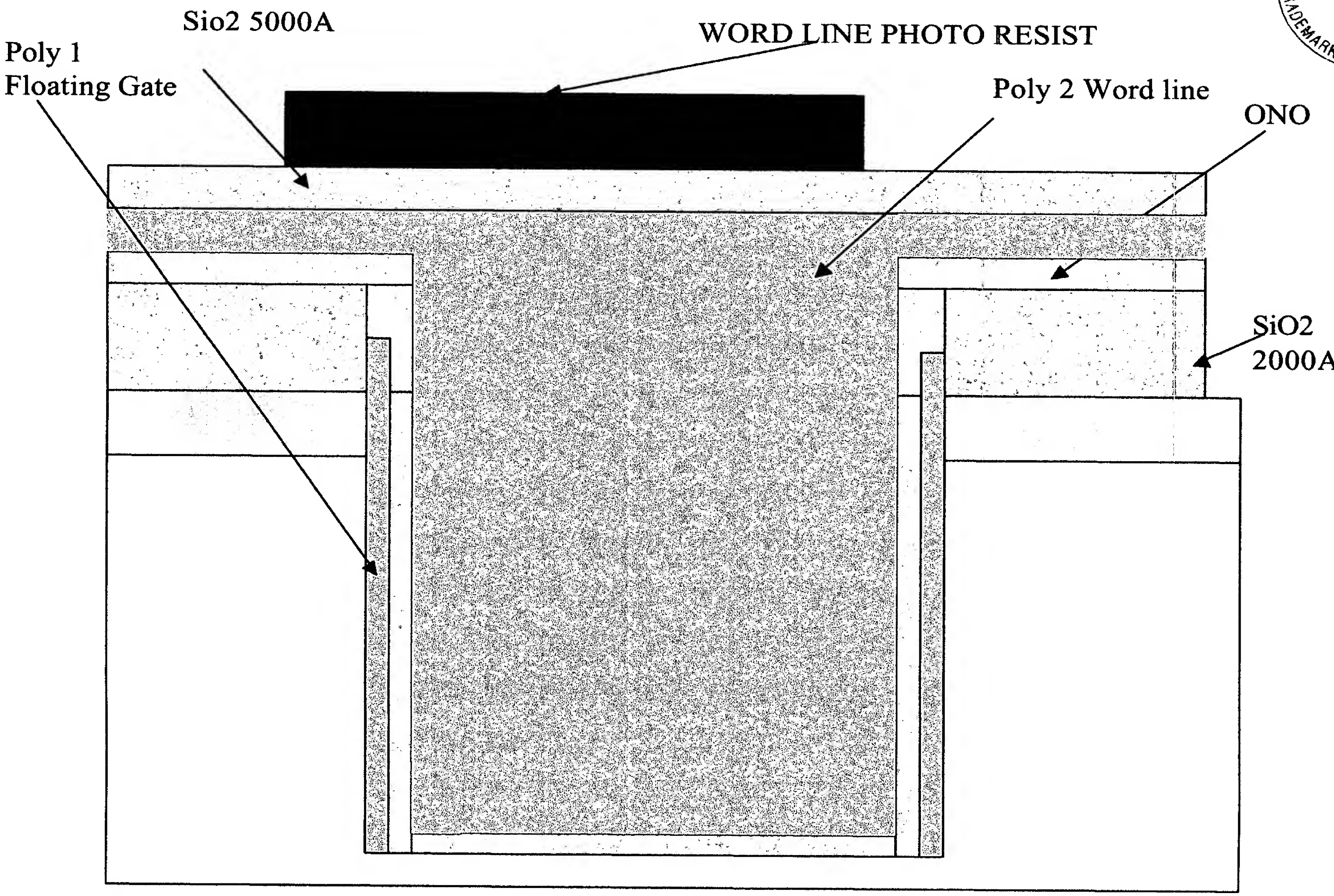


Figure 44. Cross section of Cell at AA' in Figure 2. Word line Photo resist Mis aligned .

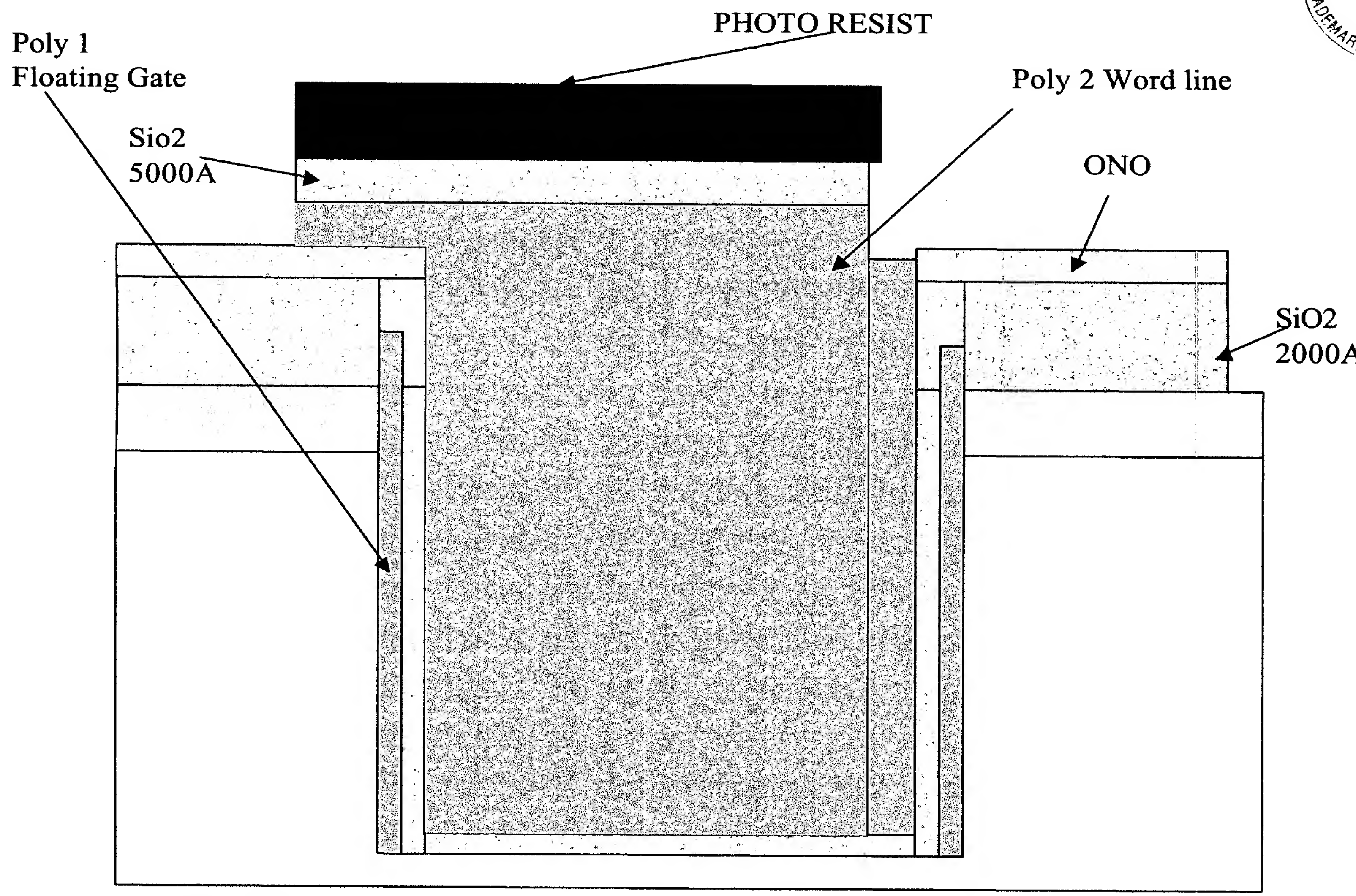


Fig.15. Oxide Etch

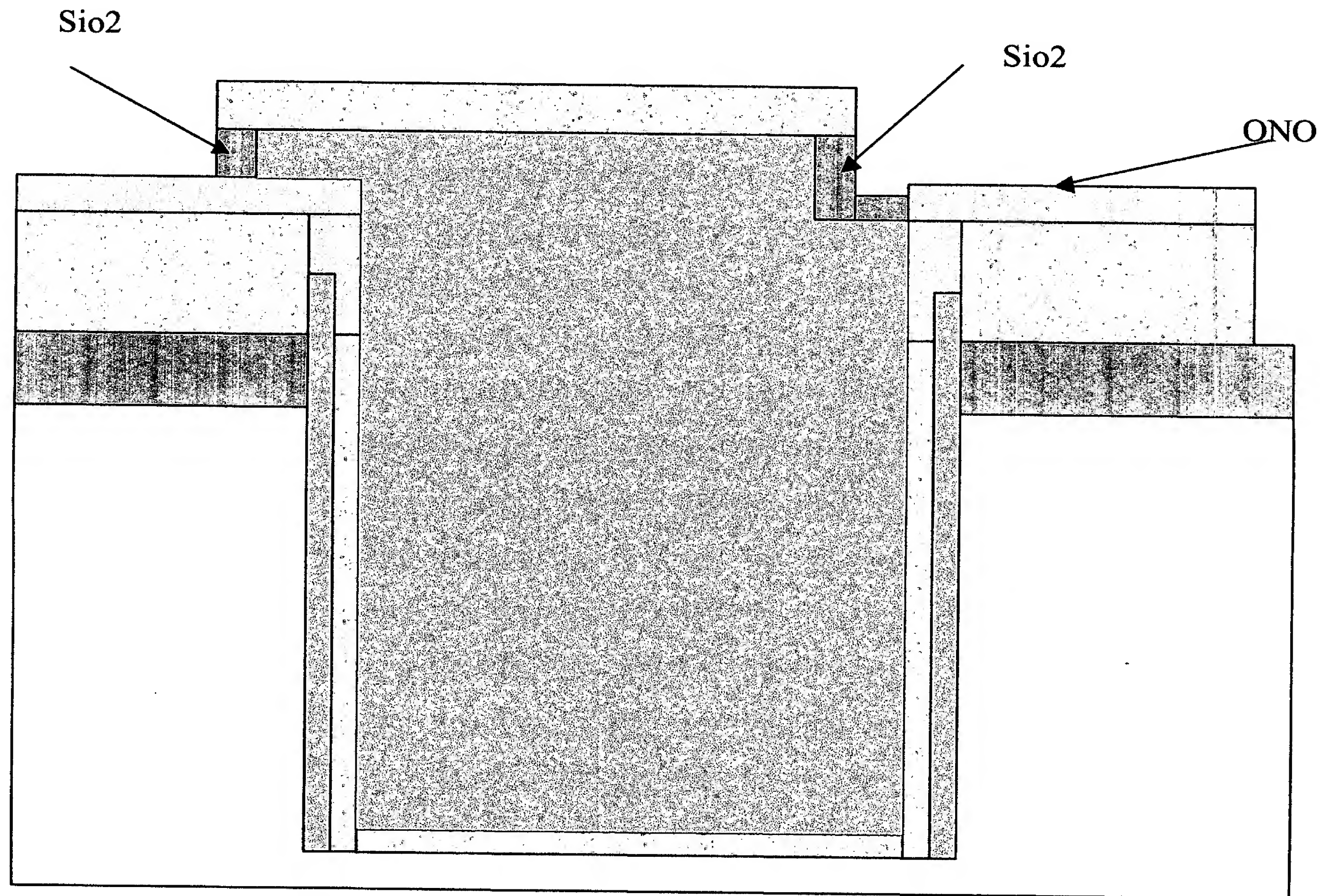


Fig. 16. Thermal Sio 2 Growth.

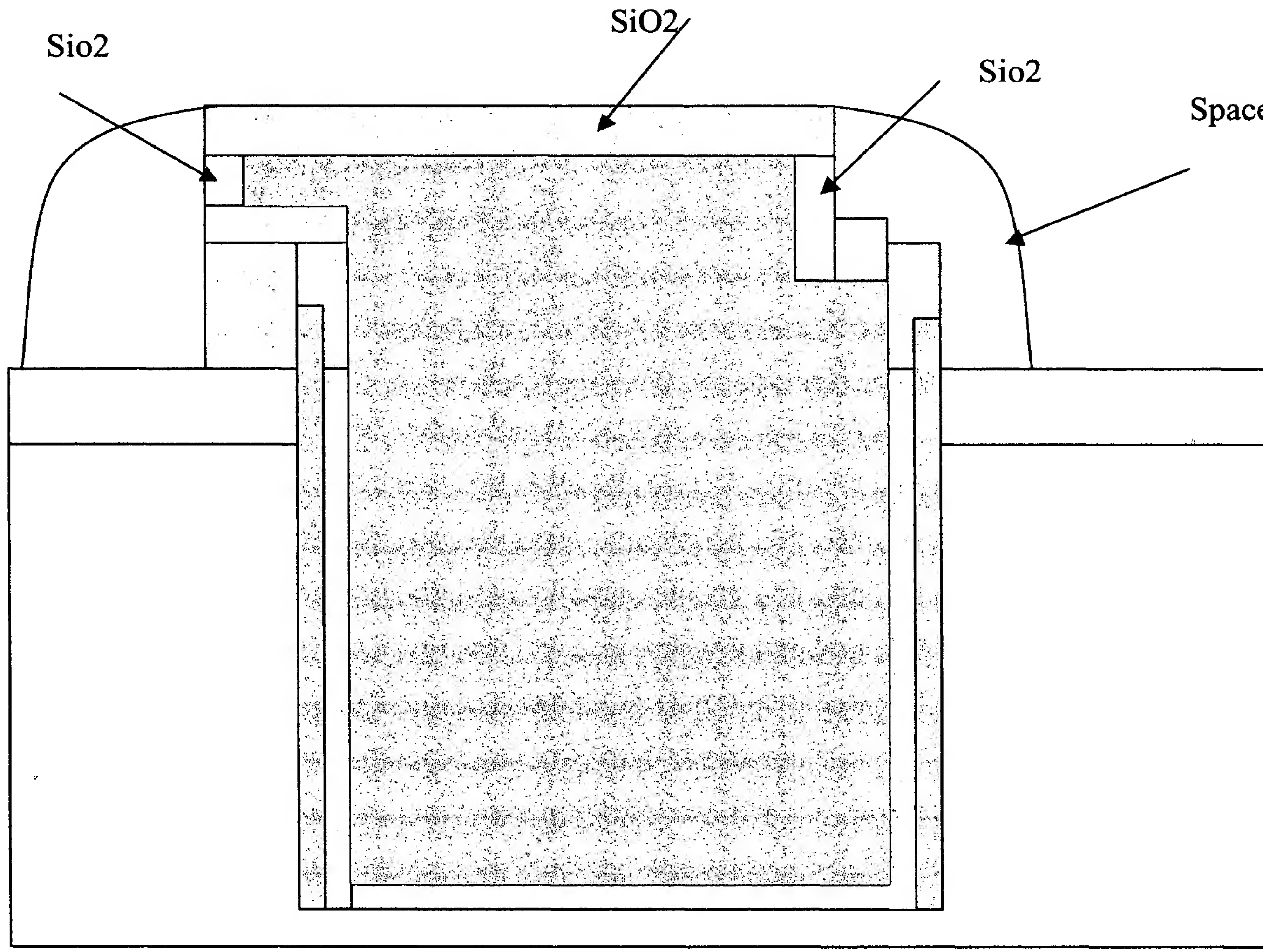


Fig1.7 ONO etch, Oxide Etch. Spacer oxide (or ONO) Deposition. Anisotropic Oxide(or ONO) etch
. to form Spacer

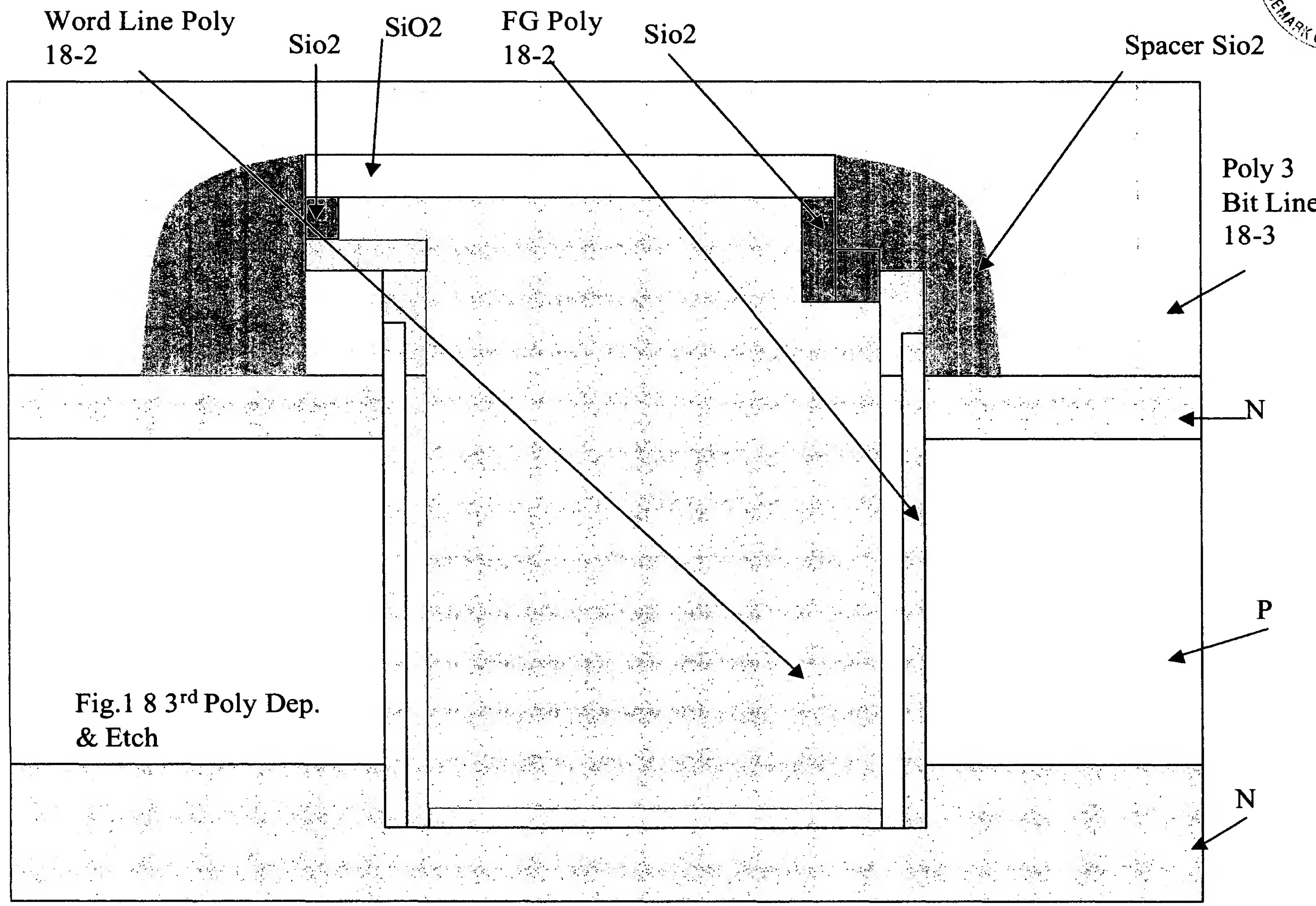


Fig.1 8 3rd Poly Dep.
& Etch

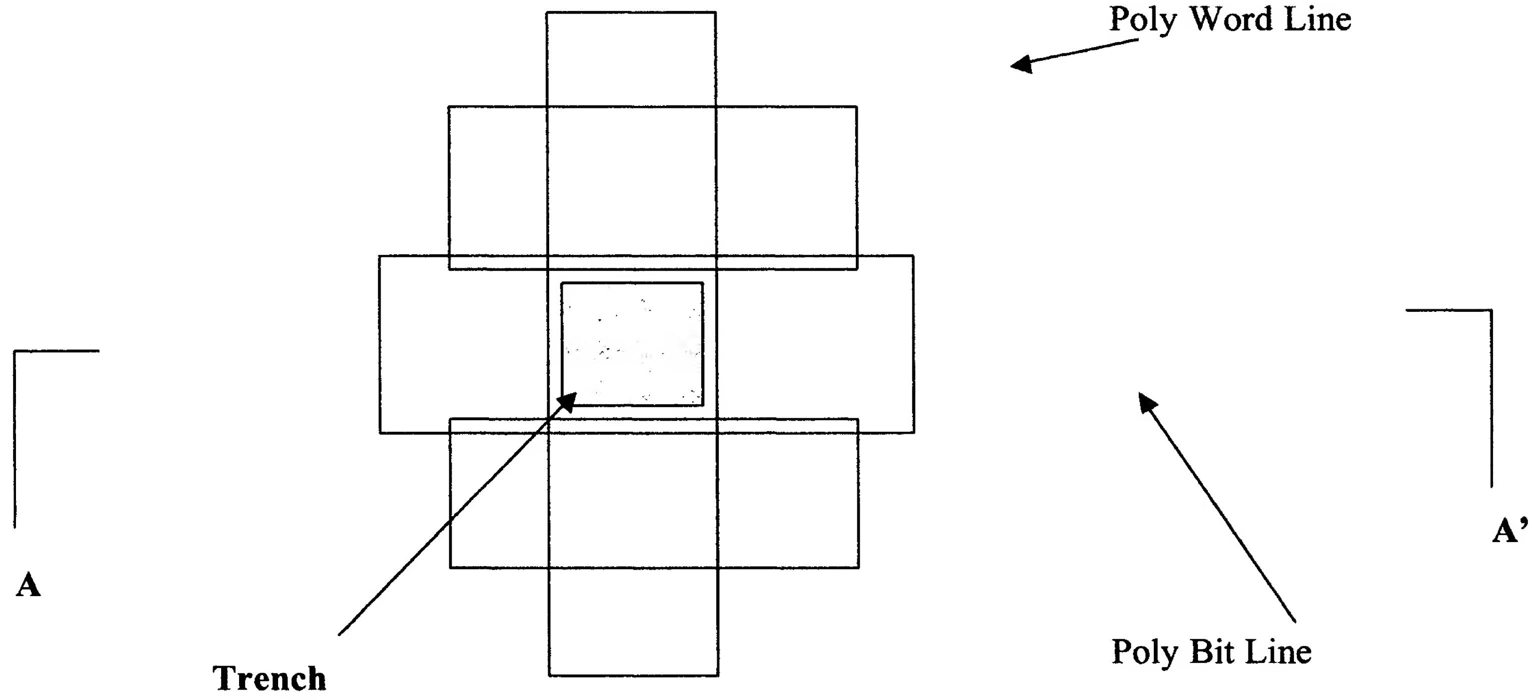


Fig 19. . Flesh EPROM Cell. Word Line   aligned with Trench.

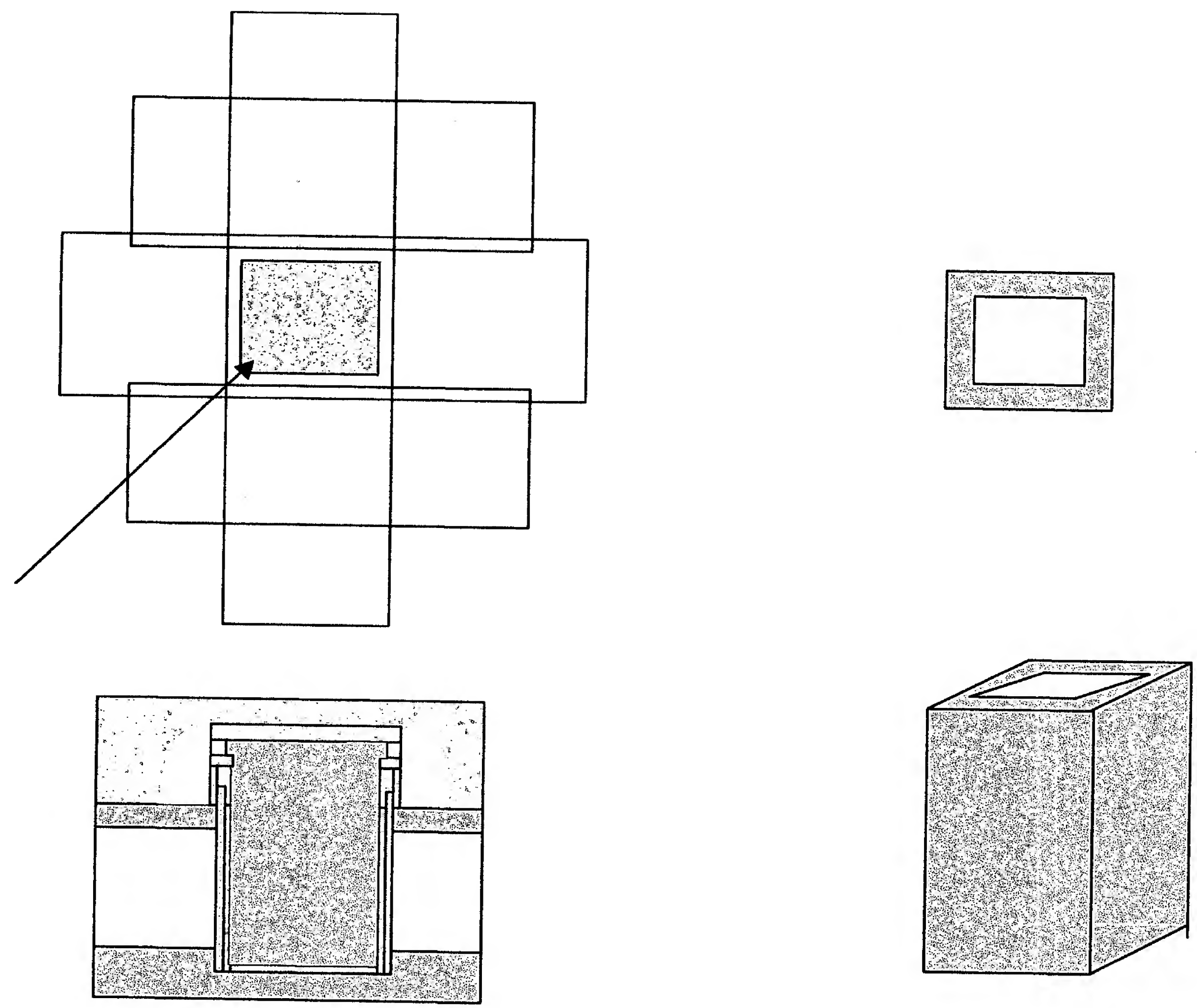
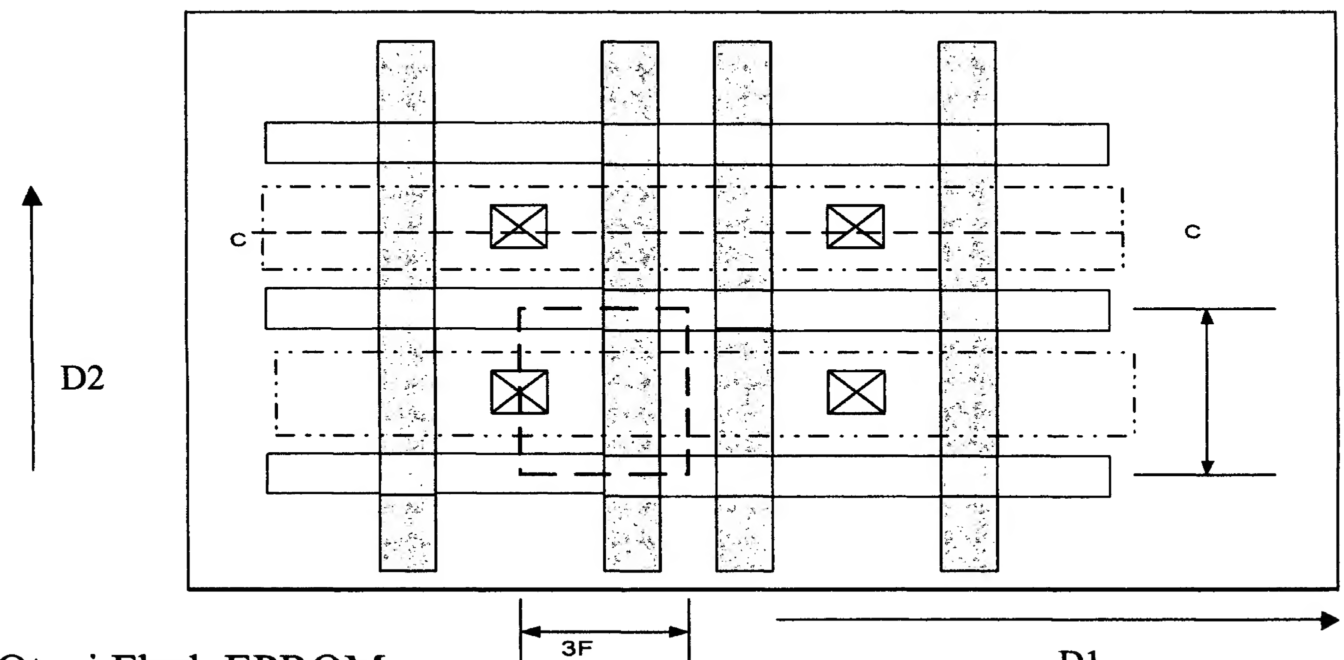


Fig. 20



Otani Flash EPROM

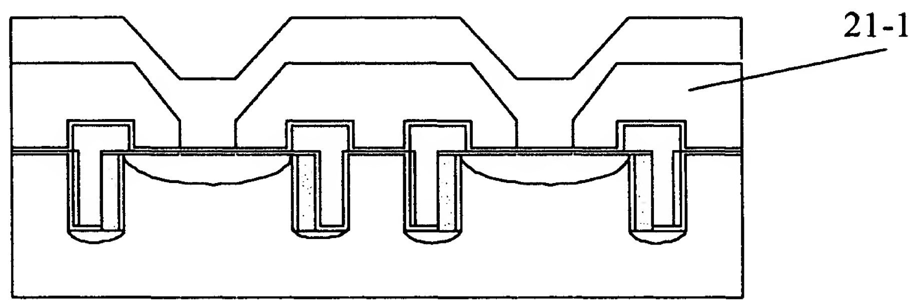


Fig 21.

Section along CC of Top View above

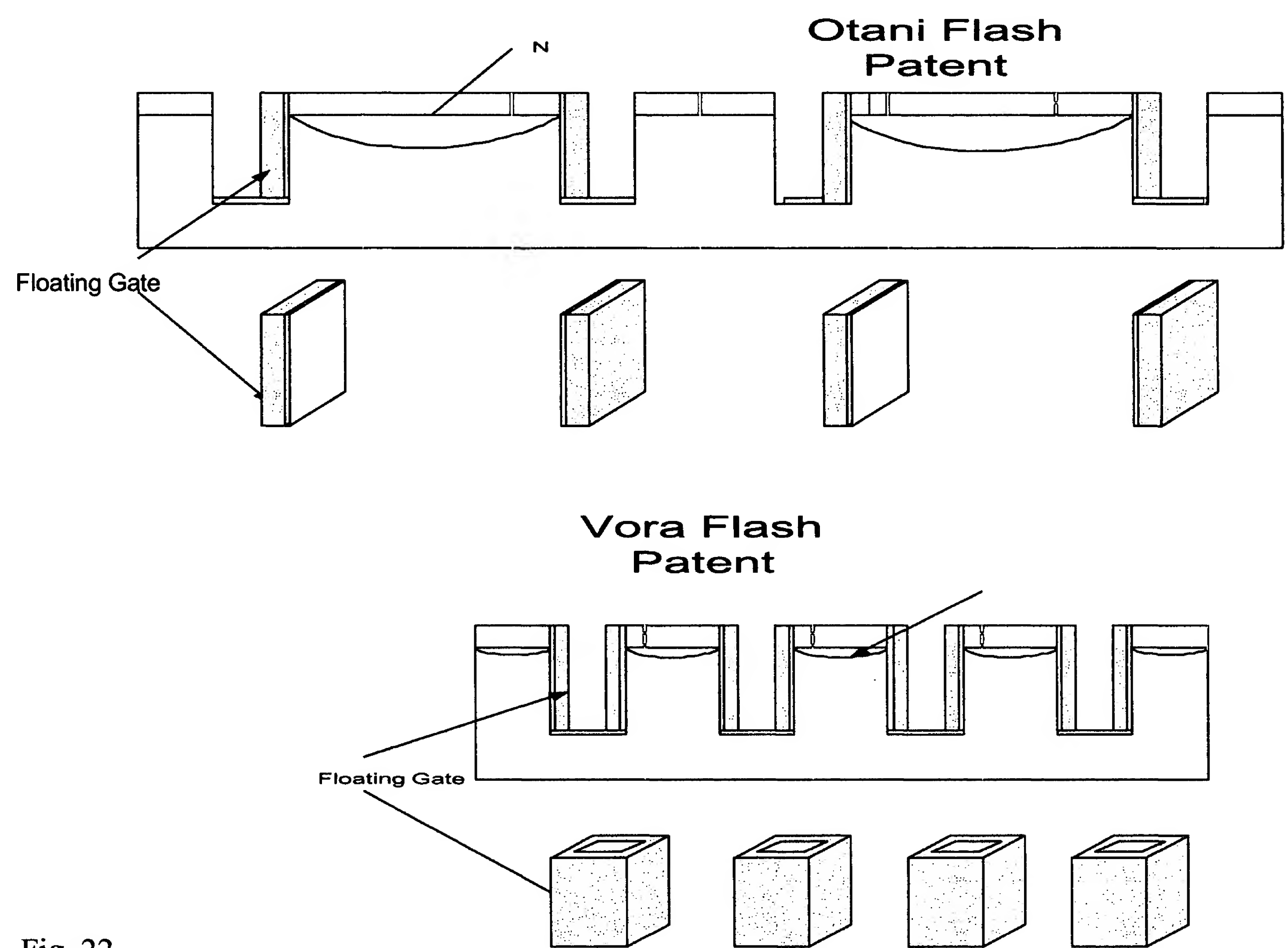

Otani Flash
Patent
N
Floating Gate
Vora Flash
Patent
Floating Gate

Fig. 22

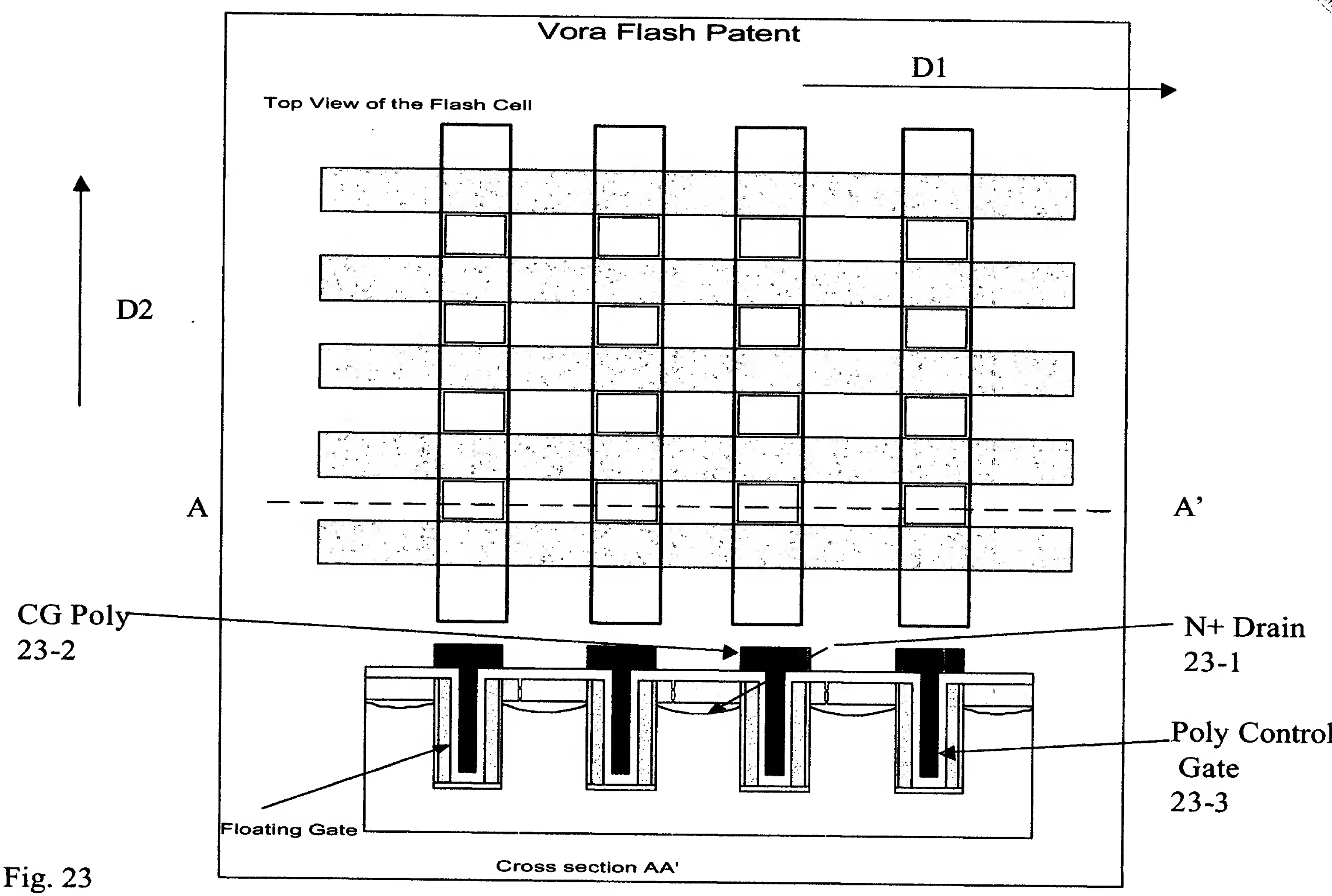

Vora Flash Patent
D1
Top View of the Flash Cell
D2
A
A'
CG Poly
23-2
N+ Drain
23-1
Poly Control
Gate
23-3
Floating Gate
Cross section AA'

Fig. 23

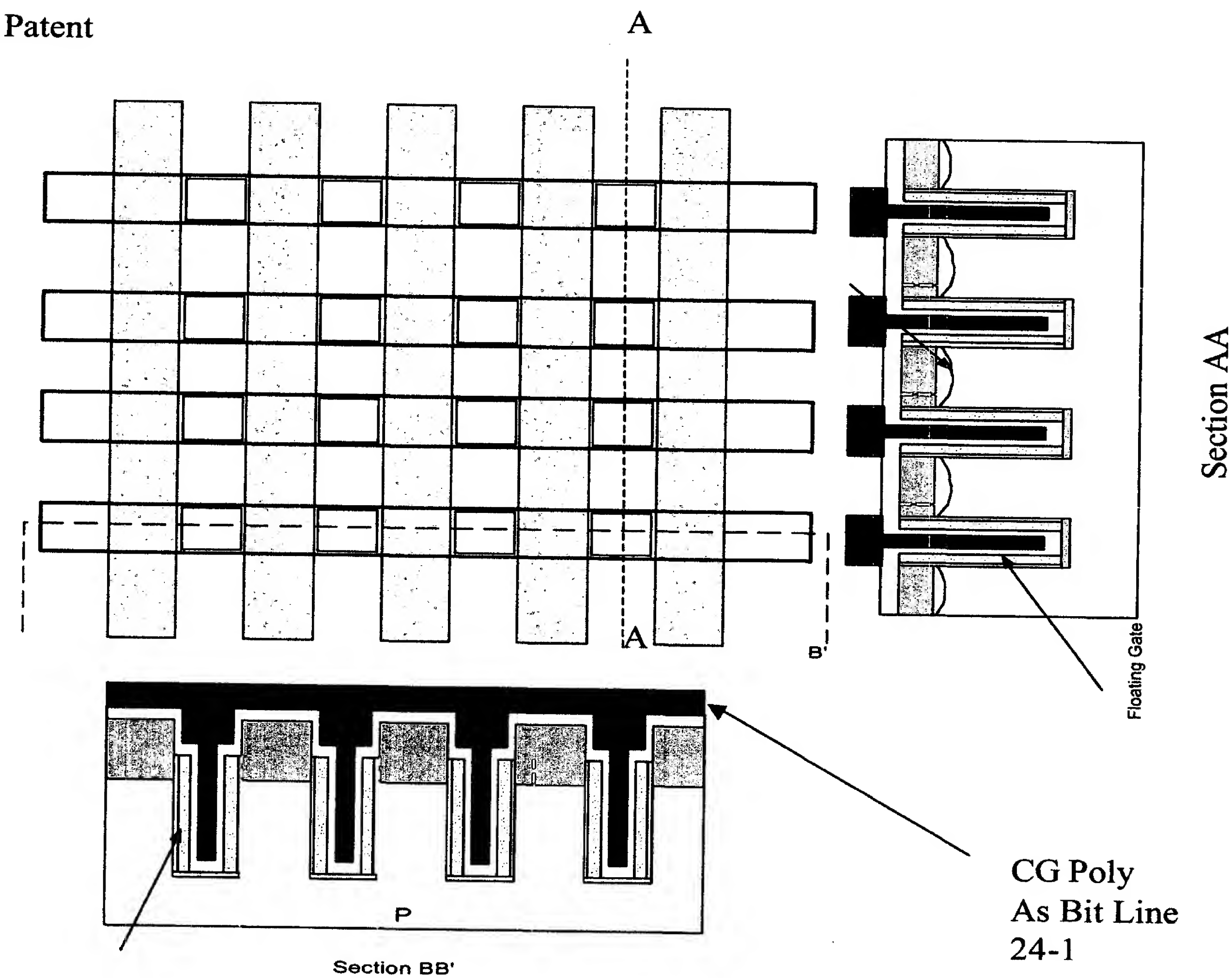
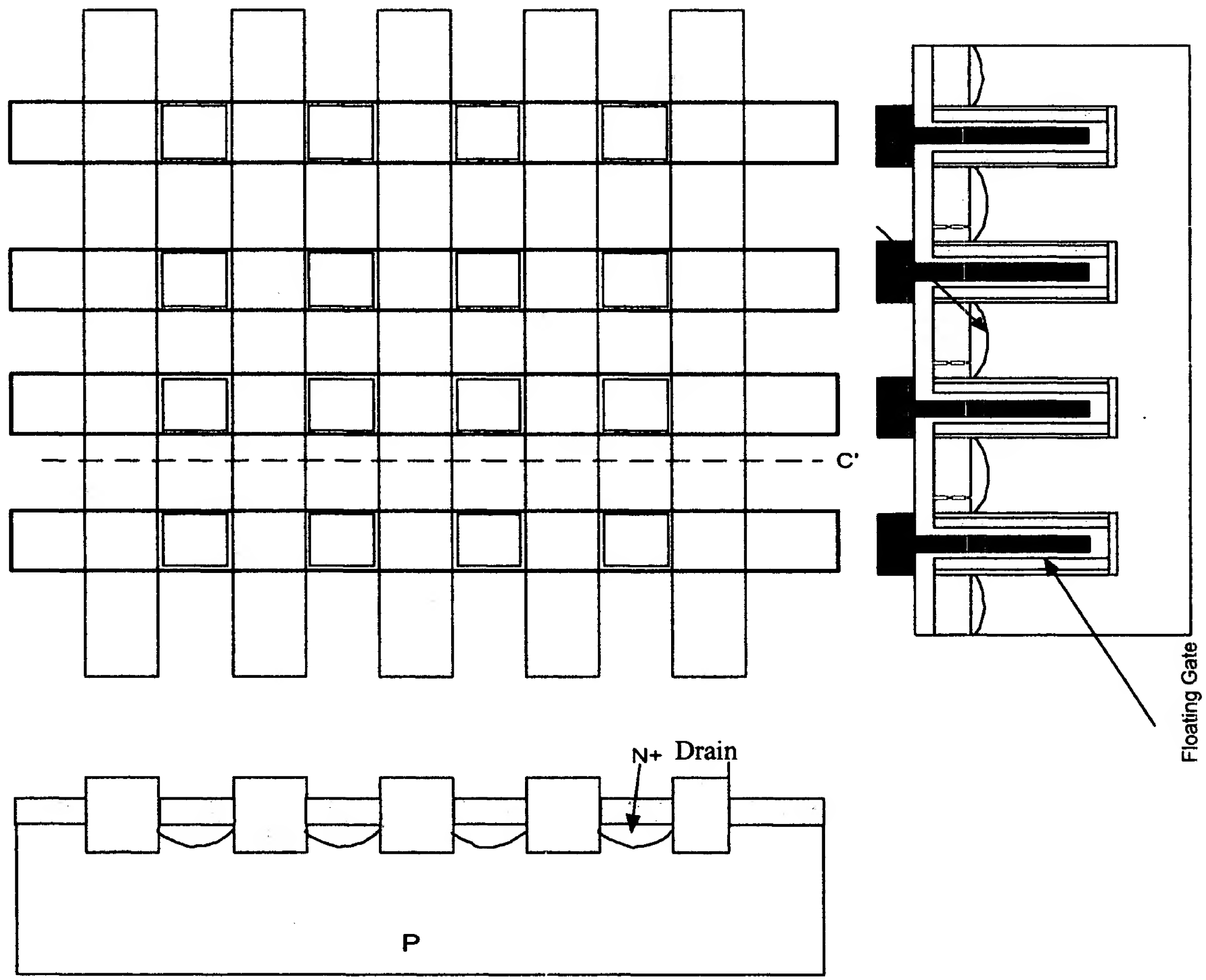

A
A
B'
Section AA
Floating Gate
P
Section BB'
CG Poly
As Bit Line
24-1

Fig. 24



Section CC'

Fig. 25